# 3250
# CRT NUMERIC CHARACTER GENERATOR
## MOS INTEGRATED CIRCUIT

**GENERAL DESCRIPTION** — The 3250 is a numeric character generator subsystem on a single chip. It is designed to be used in conjunction with a cathode ray tube to display numeric information. Deflection pulses are provided to sweep the beam through a seven segment character in eight clock pulses. Video pulses synchronized with the deflection pulses, are provided to blank the appropriate segments needed to form numerals. Approximately 520 characters may be displayed at a 60 cps refresher rate. Parallel data from a keyboard may be entered directly into the 3250 thereby simplifying systems applications.

**FEATURES:**

- **SERIAL OR PARALLEL STORAGE BUFFER ENTRY**
- **DIRECT KEYBOARD ENTRY**
- **250 kHz SEGMENT RATE**
- **BOTH HALF AND WHOLE ZEROS**
- **D/A TYPE OUTPUTS AVAILABLE FOR ±x, ±y CURRENT SUMMING AMPLIFIERS**
- **SPECIAL OUTPUTS FOR "1" OFFSET, DECIMAL POINT, AND OPTIONAL CONTROL USE**
- **INDEPENDENCE BETWEEN CHARACTER DISPLAY AND BUFFER MOTION**
- **160 mW POWER CONSUMPTION**
- **OPTIONAL CUSTOM CHARACTER SHAPES**

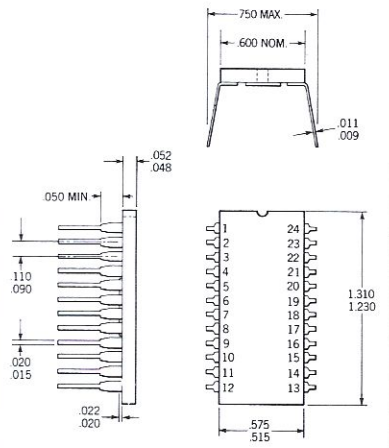
**ABSOLUTE MAXIMUM RATINGS** (above which the useful life may be impaired)

| | |
|---|---|
| All Voltages and Data Input Lines | −30 V to +0.3 V |
| Power Supply | −30 V |
| Storage Temperature | −55°C to +150°C |
| Operating Temperature (A6G325014X) | −55°C to +85°C |
| (A6G325019X) | 0°C to +70°C |

**APPLICATIONS:**

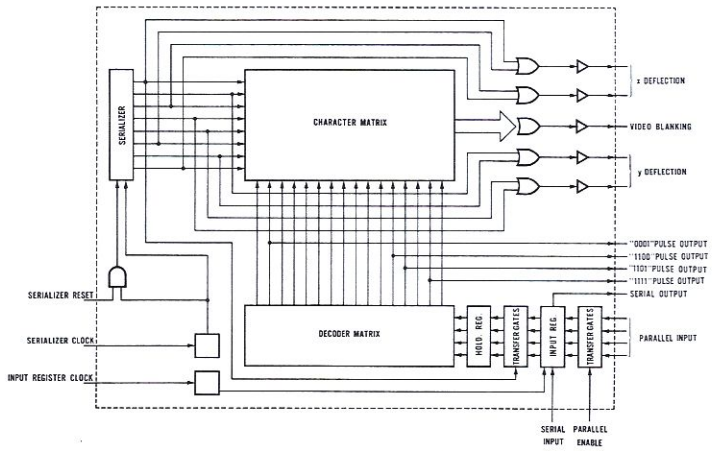
**CALCULATOR READOUTS**
**COCKPIT DISPLAYS**
**TEST EQUIPMENT READOUTS**
**DATA ACQUISITION SYSTEM READOUTS**
**NUMERICAL CONTROL MACHINE POSITION READOUTS**
**PROCESS CONTROL MONITORS**

**PHYSICAL DIMENSION**



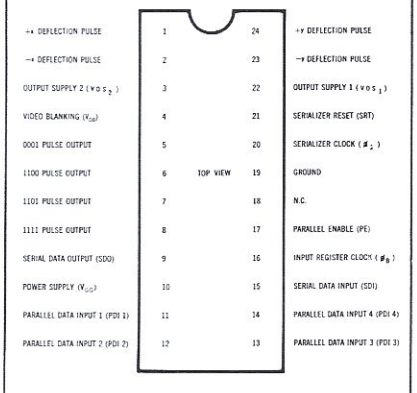

**ORDER PART NO. A6G325014X** **−55°C to +85°C**
**ORDER PART NO. A6G325019X** **0°C to 70°C**

**BLOCK DIAGRAM**




**3250 CRT NUMERIC CHARACTER GENERATOR**

**PIN CONFIGURATION**


+x DEFLECTION PULSE 1
−x DEFLECTION PULSE 2
OUTPUT SUPPLY 2 (VOS2) 3
VIDEO BLANKING (VBB) 4
0001 PULSE OUTPUT 5
1100 PULSE OUTPUT 6
1101 PULSE OUTPUT 7
1111 PULSE OUTPUT 8
SERIAL DATA OUTPUT (SDO) 9
POWER SUPPLY (VGG) 10
PARALLEL DATA INPUT 1 (PDI 1) 11
PARALLEL DATA INPUT 2 (PDI 2) 12
TOP VIEW
24 +y DEFLECTION PULSE
23 −y DEFLECTION PULSE
22 OUTPUT SUPPLY 1 (VOS1)
21 SERIALIZER RESET (SRT)
20 SERIALIZER CLOCK (ΦS)
19 GROUND
18 N.C.
17 PARALLEL ENABLE (PE)
16 INPUT REGISTER CLOCK (ΦR)
15 SERIAL DATA INPUT (SDI)
14 PARALLEL DATA INPUT 4 (PDI 4)
13 PARALLEL DATA INPUT 3 (PDI 3)

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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# FAIRCHILD MOS INTEGRATED CIRCUIT 3250

**ELECTRICAL CHARACTERISTICS** $V_{GG} = -27 \pm 1.0$ Volts, $R_L = 10$ MΩ, $C_L = 10$ pF (unless otherwise specified)

| SYMBOL | CHARACTERISTICS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| | Logic Inputs | | | | | |
| | "0" | 0 | | −2.0 | Volts | |
| | "1" | −9.0 | | −30 | Volts | |
| | Logic Outputs | | | | | |
| | "0" | 0 | | −1.0 | Volts | |
| | "1" | −10 | | −30 | Volts | |
| $\phi_S$, $\phi_B$ | Clock | | | | | |
| | Amplitude | −9.0 | | −30 | Volts | |
| $W_{cp}$ | Width | 1.0 | | 10 | μs | |
| $f_{max}$ | Segment and Input Register Frequency | DC | | 250 | kHz | |
| $C_{IN}$ | Data and Control Input Capacitance | | 7.0 | | pF | |
| $I_{max}$ | Power Supply Current Drain | | 7.5 | 9.5 | mA | $V_{GG} = -27$ V |
| $P_{max}$ | Power Dissipation | | 200 | 250 | mW | $V_{GG} = -27$ V |
| $I_{LX}$ | Input Leakage Current | | | 5.0 | μA | $V_{IN} = -20$ V |
| $t_{df}$ | Rise and Fall Times | | 1.2 | | μs | $V_{GG} = -27$ V, $f_{max} = 250$ kHz |
| $t_f$ | | | 0.4 | | μs | |
| $t_{dr}$ | | | 1.0 | | μs | |
| $t_r$ | | | 1.0 | | μs | |

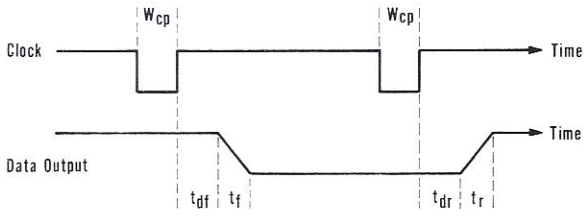
## DESCRIPTION OF PIN FUNCTIONS

| PIN | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1, 2<br>23<br>24 | −x, +x<br>−y, +y | DEFLECTION PULSES | These pulses are synchronous with the video output. When differentially integrated, they provide the deflection voltages necessary to sweep a CRT beam through the basic figure eight shape. |
| 3<br>22 | $V_{OS}$ 1 & 2 | OUTPUT SUPPLY 1 & 2 | $V_{OS}$ 1 is normally connected to ground and $V_{OS}$ 2 to −27 volts. However, for special applications, they may be connected anywhere between 0 and −27 volts. |
| 4 | VDB | VIDEO BLANKING | Video Blanking pulses, synchronous with the x & y deflections pulses, are supplied to display a character on the CRT. |
| 5, 6<br>7, 8 | | SPECIAL PURPOSE OUTPUTS | Special purpose binary codes were brought out through output buffers to be utilized for control purposes. The programmed codes may be used as follows: |
| | 0001 | | To control a "one offset" circuit which is necessary to center the character ONE within a character position. |
| | 1100<br>1111 | | To be utilized at customer option. For example a blank space for decimal point control. |
| | 1101 | | Character "A" is displayed with this code. An output is provided for external system control to be used at customer discretion. |
| 9 | SDO | SERIAL DATA OUTPUT | SDO is the LSB of the 4 bit input register. It may be connected to a larger buffer register. |
| 10 | $V_{GG}$ | POWER SUPPLY | = −27 ± 1 V. |

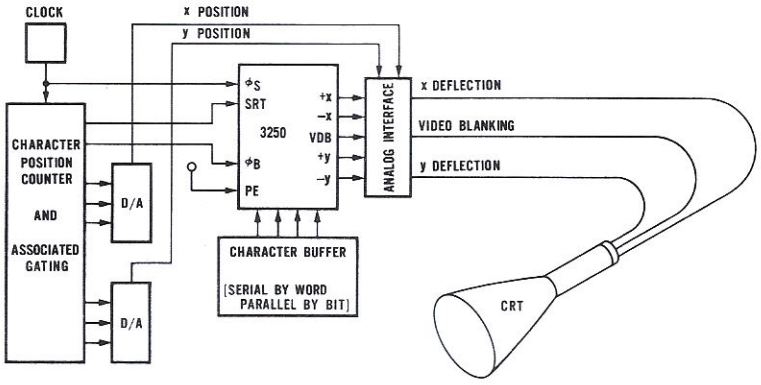
| PIN | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 11—<br>14 | PDI 1-4 | PARALLEL DATA INPUTS | Parallel data entry is provided through PDI 1-4 into the input register in synchronous with $\phi_B$ when PE is a logical "1." |
| 15 | SDI | SERIAL DATA INPUT | SDI is shifted into the MSB of the input register when PE is a logical "0" and $\phi_B$ is pulsed. |
| 16 | $\phi_B$ | INPUT REGISTER CLOCK | $\phi_B$ is utilized to control the data manipulation of the input register. (See explanation for PE below.) |
| 17 | PE | PARALLEL ENABLE | Data manipulation of the input register is synchronous with $\phi_B$ and depends upon the logical state of PE. If PE is a logical "1," the parallel inputs PDI 1-4 are loaded into the input register (PDI 4 = MSB). If PE is a logical "0," the parallel inputs are disabled and the input register operates in a serial mode. |
| 20 | $\phi_S$ | SERIALIZER CLOCK | $\phi_S$ is utilized to control the serializer. (See explanation of SRT below.) |
| 21 | SRT | SERIALIZER RESET | If SRT is a logical "0" the serializer will shift right one position when $\phi_S$ is pulsed. Zero's will be inserted into the MSB as the register shifts right. If SRT is a logical "1," then a one is inserted into the first stage and the remaining seven stages are set to zero, when $\phi_S$ is pulsed. |

## TIMING DIAGRAM

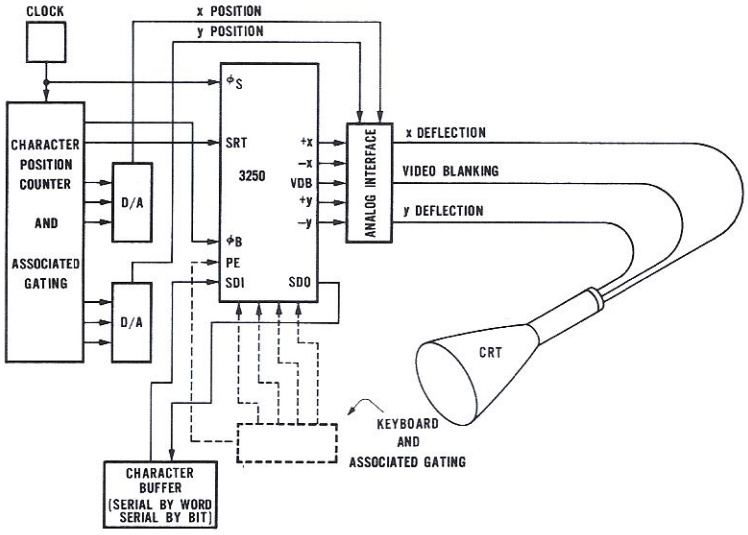
OUTPUT DELAY, RISE AND FALL TIMES



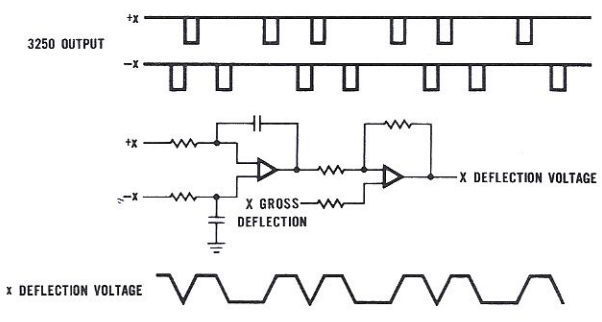
## PARALLEL BUFFER APPLICATION



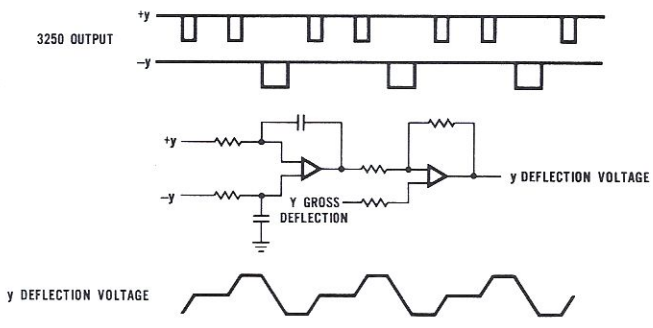

## SERIAL BUFFER APPLICATION




## DEFLECTION WAVE FORMS




SYNTHESIS OF x DEFLECTION VOLTAGE

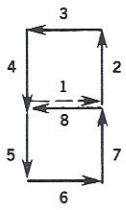



SYNTHESIS OF y DEFLECTION VOLTAGE

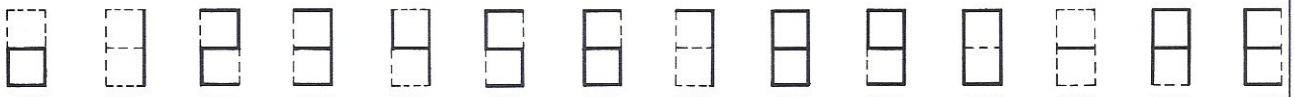
# FAIRCHILD MOS INTEGRATED CIRCUIT 3250

## CHARACTER FORMATION

A dashed line indicates a blanked segment (segment one is always blanked).



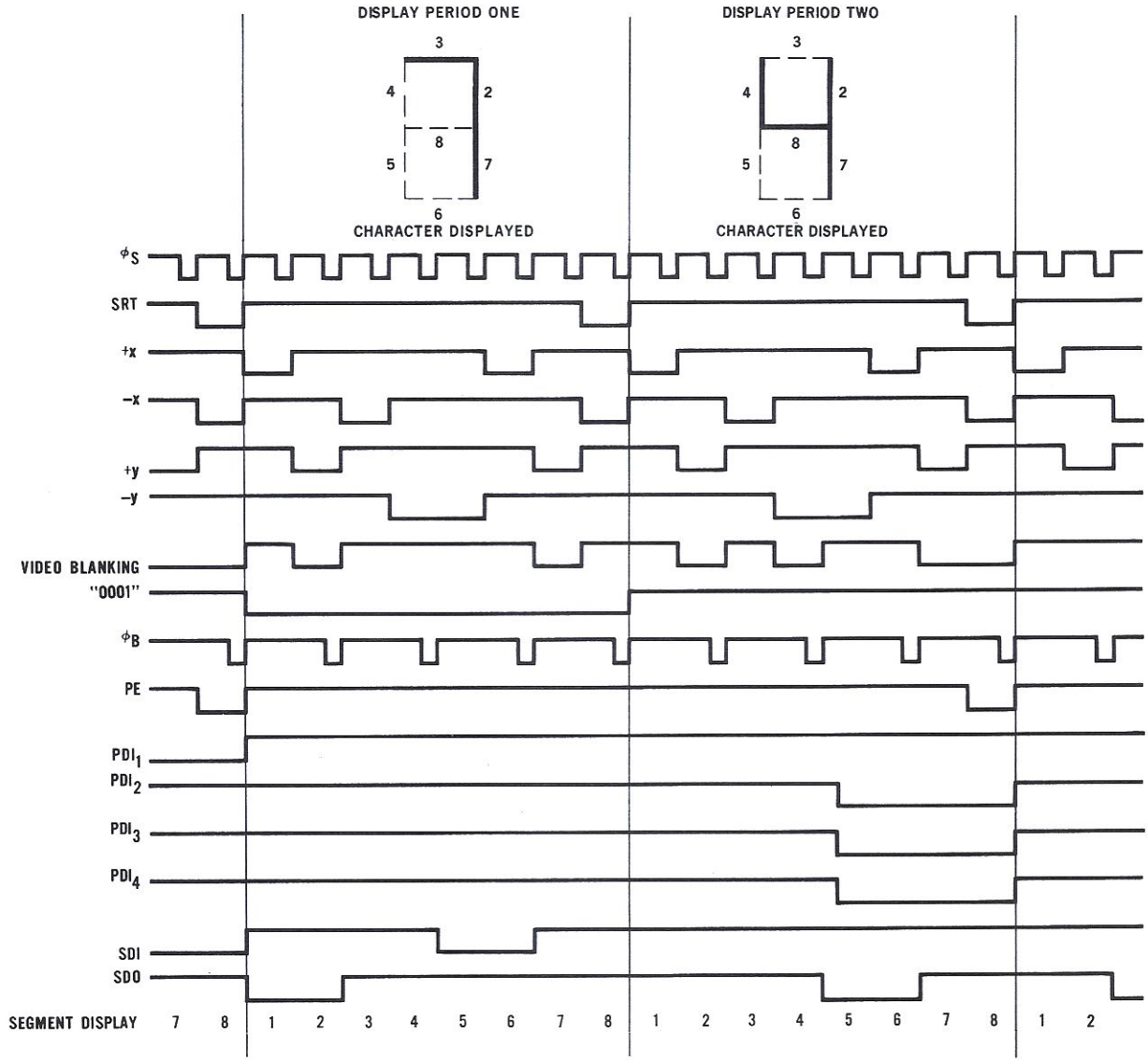

The numbers indicate the order in which segments are displayed.



| BINARY* INPUT CODE | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1101 | 1110 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

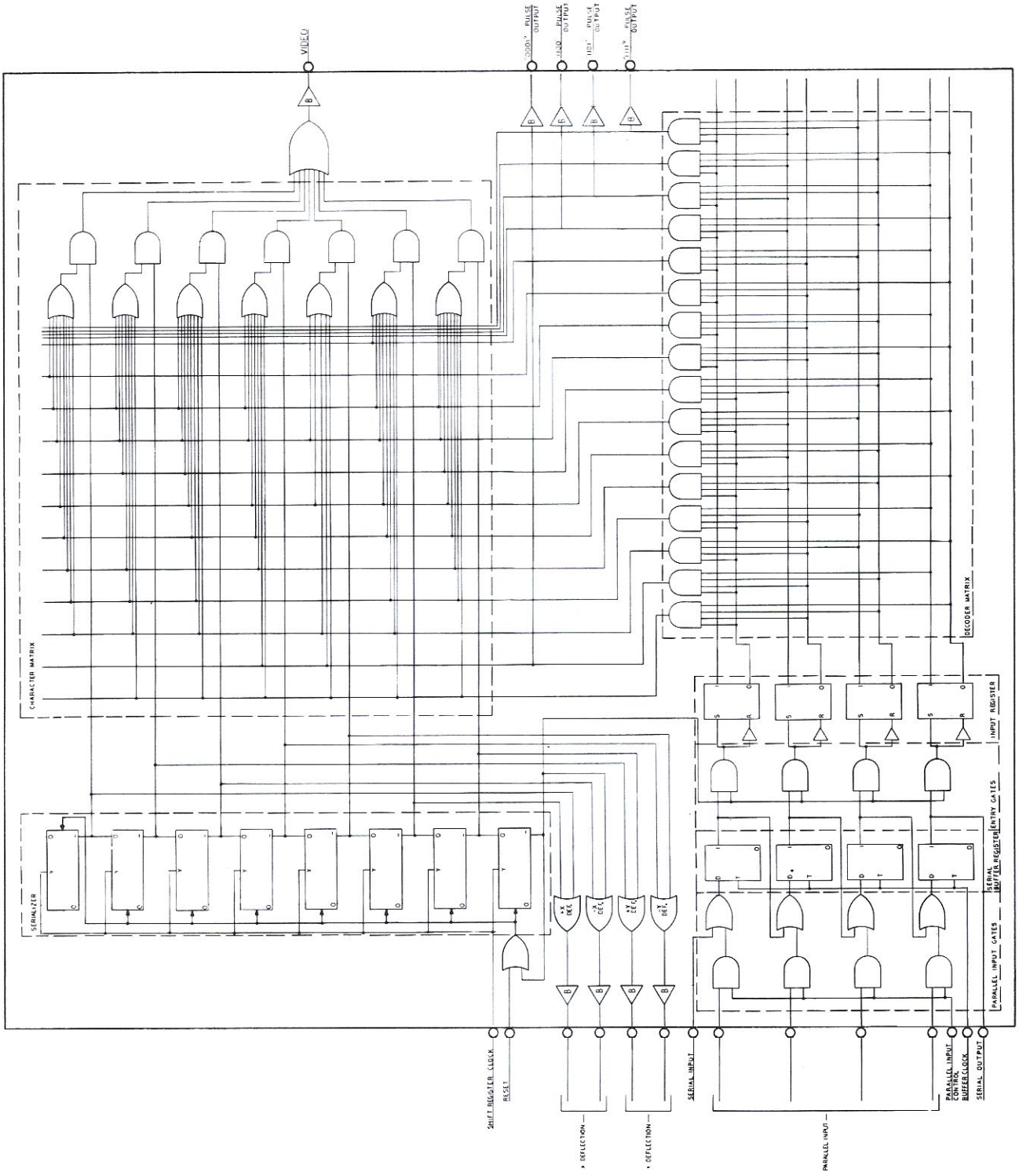
**NOTES:**
1. The "1100" and "1111" codes are used for special control purposes and create no corresponding display. Characters may be inserted into these positions for special applications.
2. See pin description for special outputs provided with 0001 and 1101 input codes.

## TYPICAL TIMING DIAGRAM




The binary data for the character displayed in period one was available for parallel loading during segment 8 of the previous period. Actual loading occurred at the fall of $\phi_B$ during segment one. The binary data for the character displayed during display period two was loaded serially during display period one. The input data must not change during segment two of any display period.

## LOGIC BLOCK DIAGRAM




NOTE: Polarity indicators (○) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈ −10 V and 1.0 = "0" ≈ Gnd.

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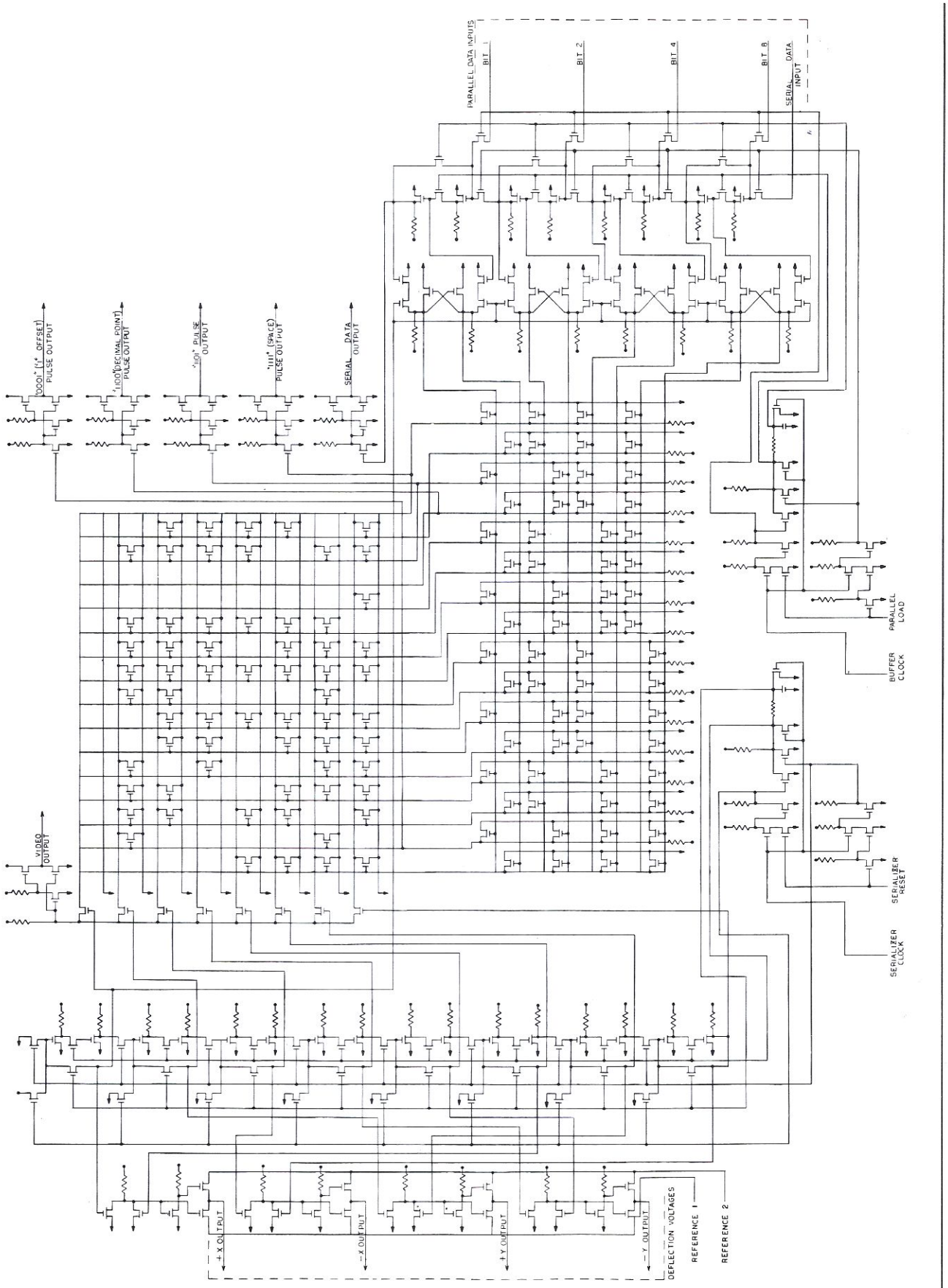
## CIRCUIT DIAGRAM

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